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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,244	03/23/2004	Motohiro Enkaku	250923US2S	1778

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EXAMINER	
RADOSEVICH, STEVEN D	
ART UNIT	PAPER NUMBER
2117	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/26/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 04/26/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/806,244	ENKAKU, MOTOHIRO	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/04/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/26/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-19 are present for this examination.

Priority

Foreign priority for this case is 08/29/2003.

Information Disclosure Statement

Acknowledgement is made that an IDS was provided after the First Office Action on 12/26/2006 identifying three foreign Japanese patent documents without translations. These documents will be given consideration within this instant application.

Drawings

The drawings (4-6) remain objected to since applicant's remarks fail to explain the deficiencies the examiner indicated within the prior examination. Applicant directed the examiner to page 15 of the specification with specific attention to lines 5-17 in an attempt to reveal what "n" and "k" are representative of within the drawings (4-6). The specification does not disclose what "n" and "k" are representative of other they are some number without reference as to what that number is a representative of other then when divided by two equal to an even number. It is unclear what numerical value "n" and "k" are representative of from either the specification or the figures. Applicant is requested to indicate what circuitry, components, elements, or what "n" and "k" are representative of.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 11, and 15, are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: testing the information programmed within the programmable circuit before initiating a correction process of transferring information within the programmable circuit to the information holding circuit when the information held in the information holding circuit is detected as destroyed. Examiner notes that the expected value information is not dependent upon the information programmed within the programmable circuit as the claims are written; the data within the programmable circuit itself may be in error.

Claims 10-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 10, 14, and 18, each of these claims recites the imitation, "an information output circuit which outputs expected value correcting information used to correct compression information compressed by the information compression circuit to expected value information." It is unclear to the examiner why the compressed information it being corrected and where within the specification this limitation is supported. Appropriate correction or explanation is required for understanding.

Claims 11-13, 15-17, and 19 are dependent upon claims 10, 14, and 18 respectively and therefore also inherit the 35 U.S.C. 112, second paragraph issues of the independent claims and may not be further considered on their merits.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakano Takashi (Japanese Publication 09-282237).

1. As per claim 1, Nakano teaches a semiconductor integrated circuit device comprising:

A programmable circuit in which information is program (see abstract);

An information holding circuit which electronically holds information programmed in the programmable circuit (see abstract);

A compression circuit which compresses information held in the information holding circuit (see abstract);

An information output circuit which outputs expected value information (see abstract); and

A detecting circuit which compares the expected value information with compression information of the information compression circuit to check destruction of information held in the information holding circuit (see abstract).

2. As per claim 2, the device further comprising a correction process execution circuit which executes a correction process for information held in the information

holding circuit when it is detected that the information is destroyed (see abstract - rewrites the storage data).

3. As per claim 10, Nakano teaches a semiconductor integrated circuit device comprising:

A programmable circuit in which information is programmed (see abstract);

An information holding circuit which electronically holds information programmed in the programmable circuit (see abstract);

A compression circuit which compresses information held in the information holding circuit (see abstract);

An information output circuit which outputs expected value correcting information used to correct compression information compressed by the information compression circuit to expected value information (see abstract);

An expected value correction circuit which outputs the expected value information based on the compression information and expected value correction (see abstract); and

Correction information process execution circuit which executes a correction process for information held in the information holding circuit when it is detected that the information is destroyed, destruction of information stored in the information holding circuit being checked based on a variation in the expected value information (see abstract).

4. As per claim 14, Nakano teaches a semiconductor integrated circuit device comprising:

A programmable circuit in which information is programmed (see abstract);

An information holding circuit which electronically holds information programmed in the programmable circuit (see abstract);

A compression circuit which compresses information held in the information holding circuit (see abstract); and

A correction process execution circuit which executes a correction process for information held in the information holding circuit when it is detected that information is destroyed, destruction of information stored in the information holding circuit being checked based on a variation in the expected value information (see abstract).

5. As per claim 18, Nakano teaches a semiconductor integrated circuit device comprising:

A programmable circuit in which information is programmed (see abstract);

An information holding circuit which electronically holds information programmed in the programmable circuit (see abstract);

A compression circuit which compresses information held in the information holding circuit (see abstract); and

An information output circuit which outputs expected value correction information used to correct compression information compressed by the information compression circuit to expected value information (see abstract);

Wherein destruction of information stored in the information holding circuit is checked based on a variation in the expected value information and the information output circuit includes an expected value correcting information generating circuit which generates expected value correcting information and the expected value correcting information generating circuit compresses information programmed in the programmable circuit to generate expected value correcting information when the programmed information is held in the information holding circuit (see abstract)

6. As per claims 3, 11, and 15, Nakano teaches the device wherein the correction process is a process to transfer information programmed in the programmable circuit to the information holding circuit (see abstract – rewrites).

7. As per claims 4, 12, and 16, the device further comprising a mirror-ring information holding circuit configured by connecting the information holding circuit in a mirror-ring form, wherein the correction process is a process in which information is mutually transferred between the information holding circuit and the mirror-ring information holding circuit to make information held in the information holding circuit coincident with information held in the mirror-ring information holding circuit (see abstract – mirror)

8. As per claims 5, 13, and 17, Nakano teaches the device further comprising an IP macro which uses information held in the information holding circuit, and a status information generating circuit which generates status information indicating the status of the IP macro, wherein the correction process execution circuit suspends a system containing the IP macro when the IP macro is set in a non-active status and resets the system containing the IP macro when the IP macro is set in an active status (see abstract).

9. As per claim 6, Nakano teaches the device wherein the information output circuit includes an expected value information generating circuit which generates expected value information and the expected value information generating circuit compresses information programmed in the programmable circuit to generate expected value information when the programmed information is held in the information holding circuit (see abstract).

10. As per claims 7, Nakano teaches the device wherein the compression process is an accumulation addition process (see abstract).

11. As per claim 19, Nakano teaches the device wherein the compressing process is and accumulative addition process (see abstract - check sum).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
PRIMARY EXAMINER
AU 2138

Steven D. Radosevich
Examiner
Art Unit 2138